FIG.1

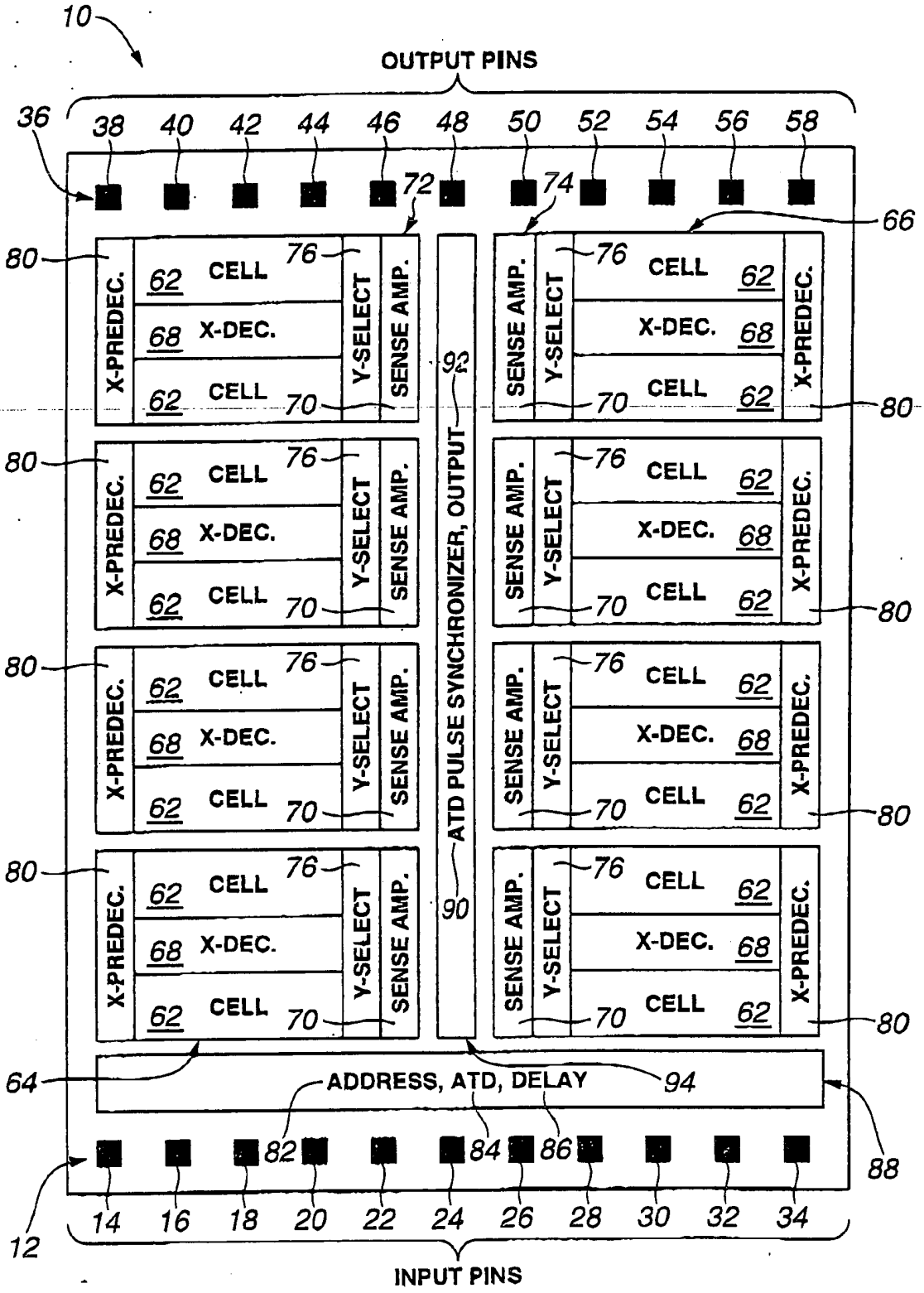

10
OUTPUT PINS
36
38
40
42
44
46
48
50
52
54
56
58
72
74
66
80
X-PREDEC.
62
CELL
76
68
X-DEC.
Y-SELECT
SENSE AMP.
70
92
ATD PULSE SYNCHRONIZER, OUTPUT
90
64
ADDRESS, ATD, DELAY
94
82
84
86
88
12
14
16
18
20
22
24
26
28
30
32
34
INPUT PINS

FIG.2

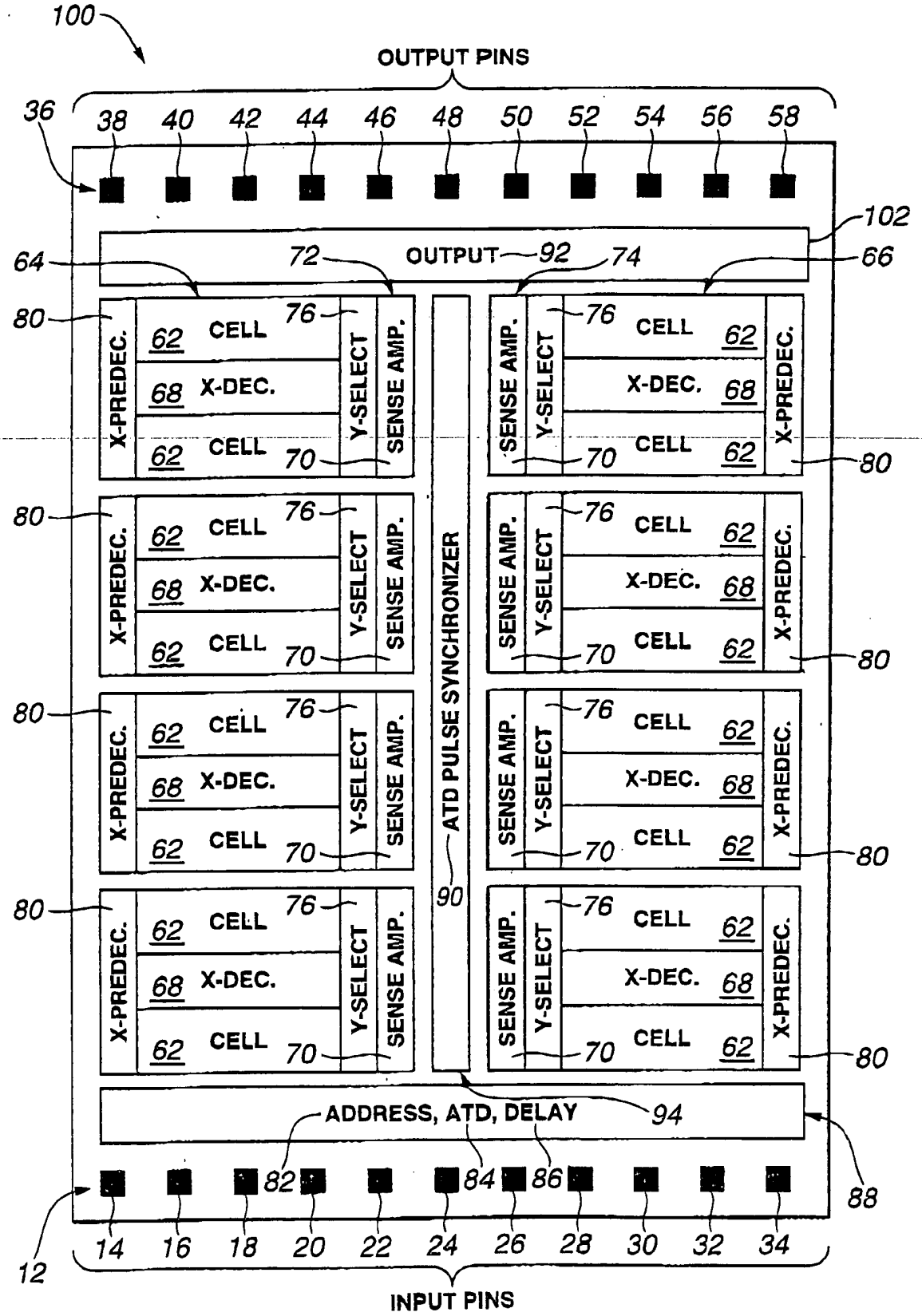

100
OUTPUT PINS
36
38
40
42
44
46
48
50
52
54
56
58
102
64
72
OUTPUT
92
74
66
80
X-PREDEC.
62
CELL
76
68
X-DEC.
Y-SELECT
SENSE AMP.
70
ATD PULSE SYNCHRONIZER
90
ADDRESS, ATD, DELAY
94
82
84
86
88
12
14
16
18
20
22
24
26
28
30
32
34
INPUT PINS

FIG.3

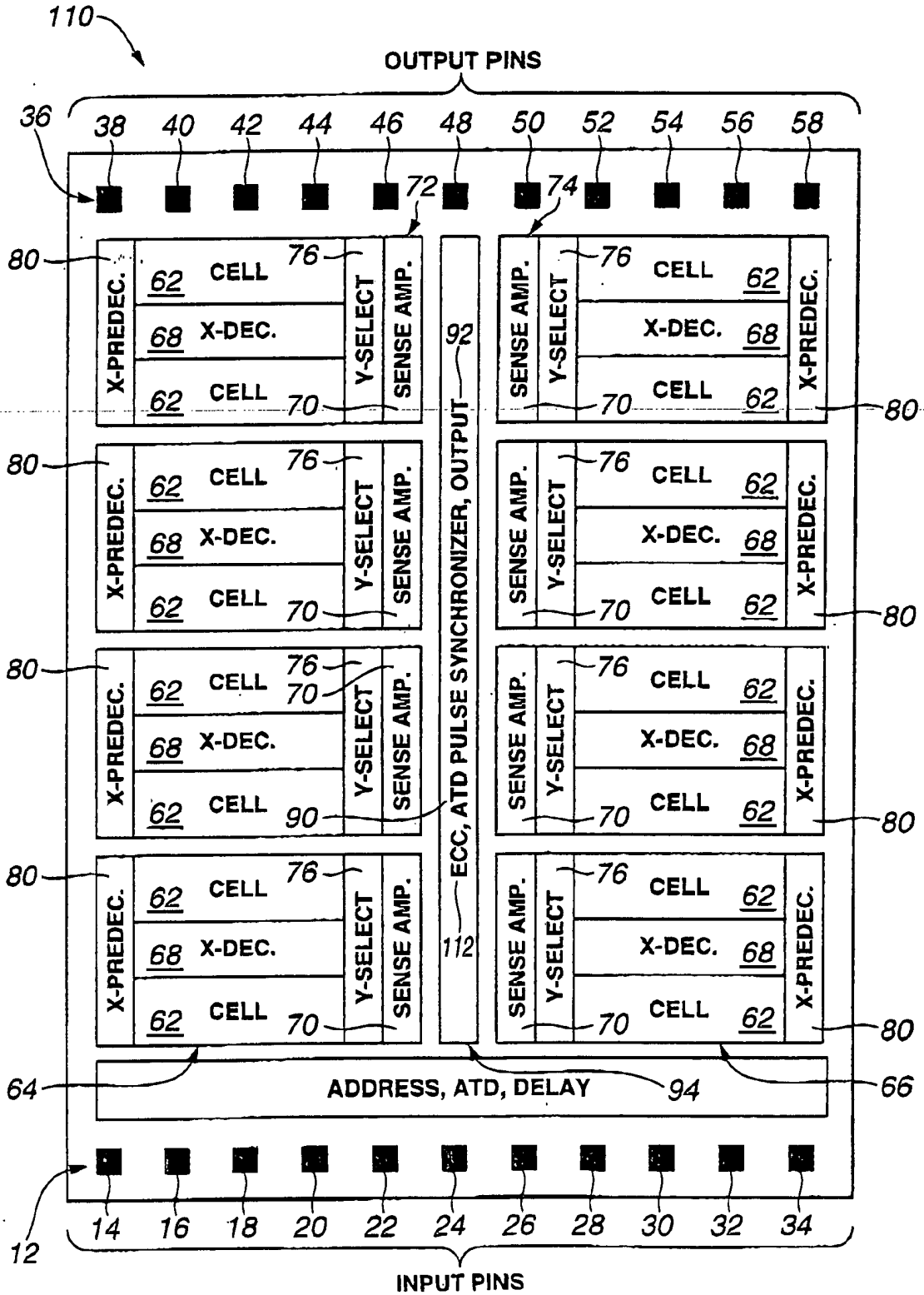

110
OUTPUT PINS
36
38
40
42
44
46
48
50
52
54
56
58
72
74
80
X-PREDEC.
62
CELL
76
68
X-DEC.
Y-SELECT
SENSE AMP.
70
92
ECC, ATD PULSE SYNCHRONIZER, OUTPUT
90
112
64
ADDRESS, ATD, DELAY
94
66
12
14
16
18
20
22
24
26
28
30
32
34
INPUT PINS

FIG.4

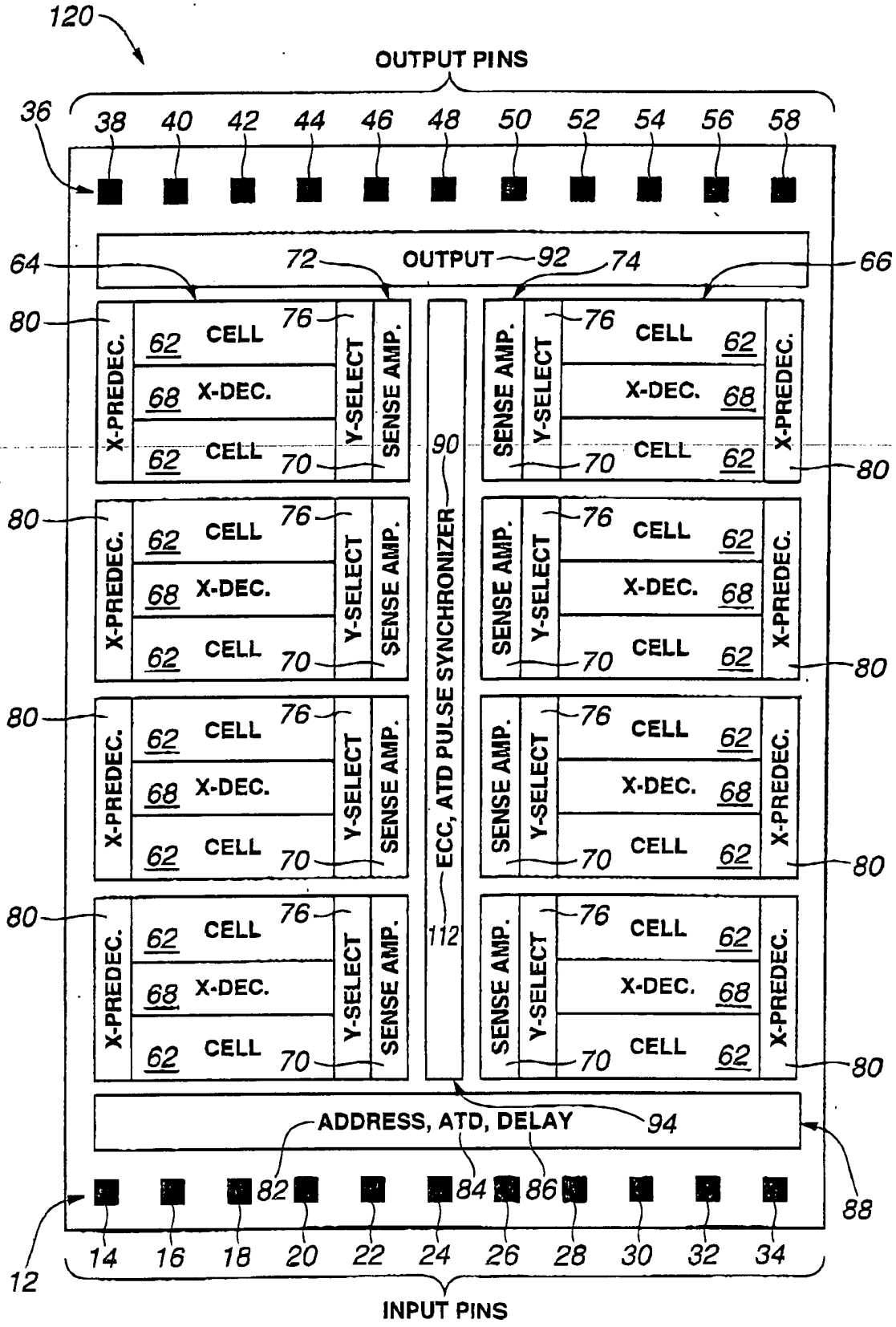

120
OUTPUT PINS
36
38
40
42
44
46
48
50
52
54
56
58
64
72
OUTPUT
92
74
66
80
X-PREDEC.
62
CELL
76
68
X-DEC.
70
Y-SELECT
SENSE AMP.
90
ECC, ATD PULSE SYNCHRONIZER
112
ADDRESS, ATD, DELAY
94
82
84
86
88
12
14
16
18
20
22
24
26
28
30
32
34
INPUT PINS

FIG.5

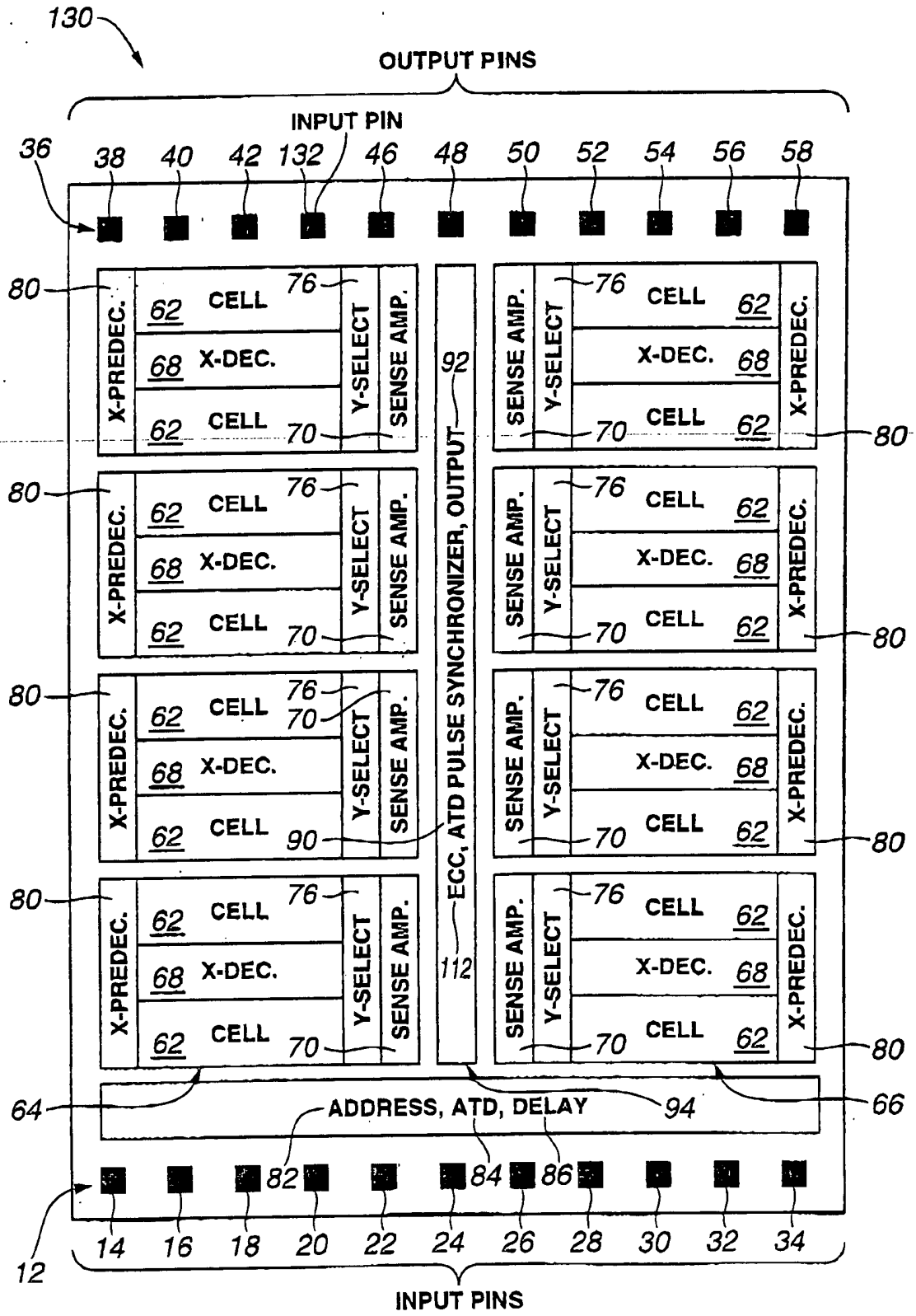

130
OUTPUT PINS
INPUT PIN
36
38
40
42
132
46
48
50
52
54
56
58
80
X-PREDEC.
62
CELL
76
68
X-DEC.
Y-SELECT
SENSE AMP.
70
92
ECC, ATD PULSE SYNCHRONIZER, OUTPUT
90
112
64
ADDRESS, ATD, DELAY
94
66
82
84
86
12
14
16
18
20
22
24
26
28
30
32
34
INPUT PINS

FIG.6

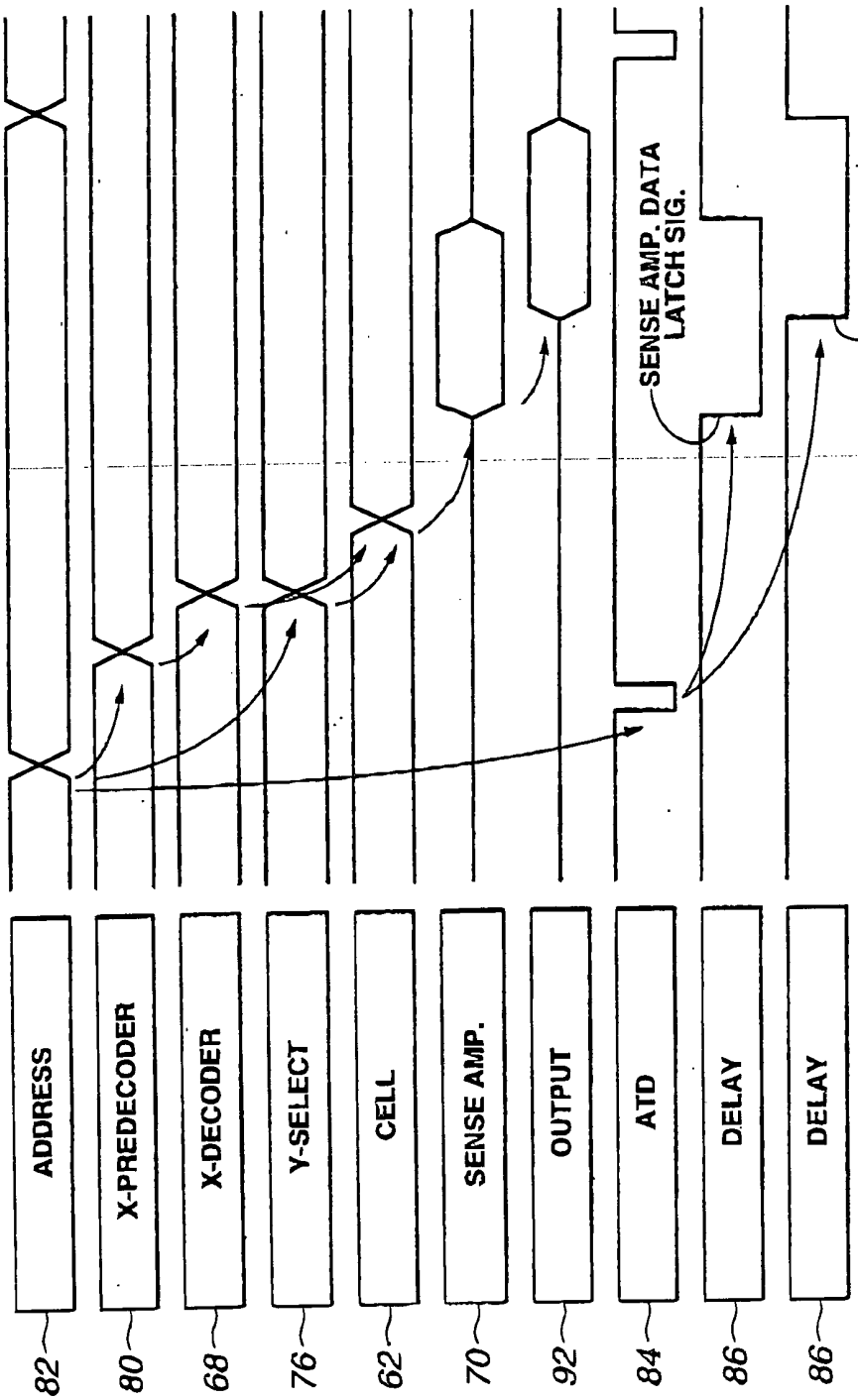
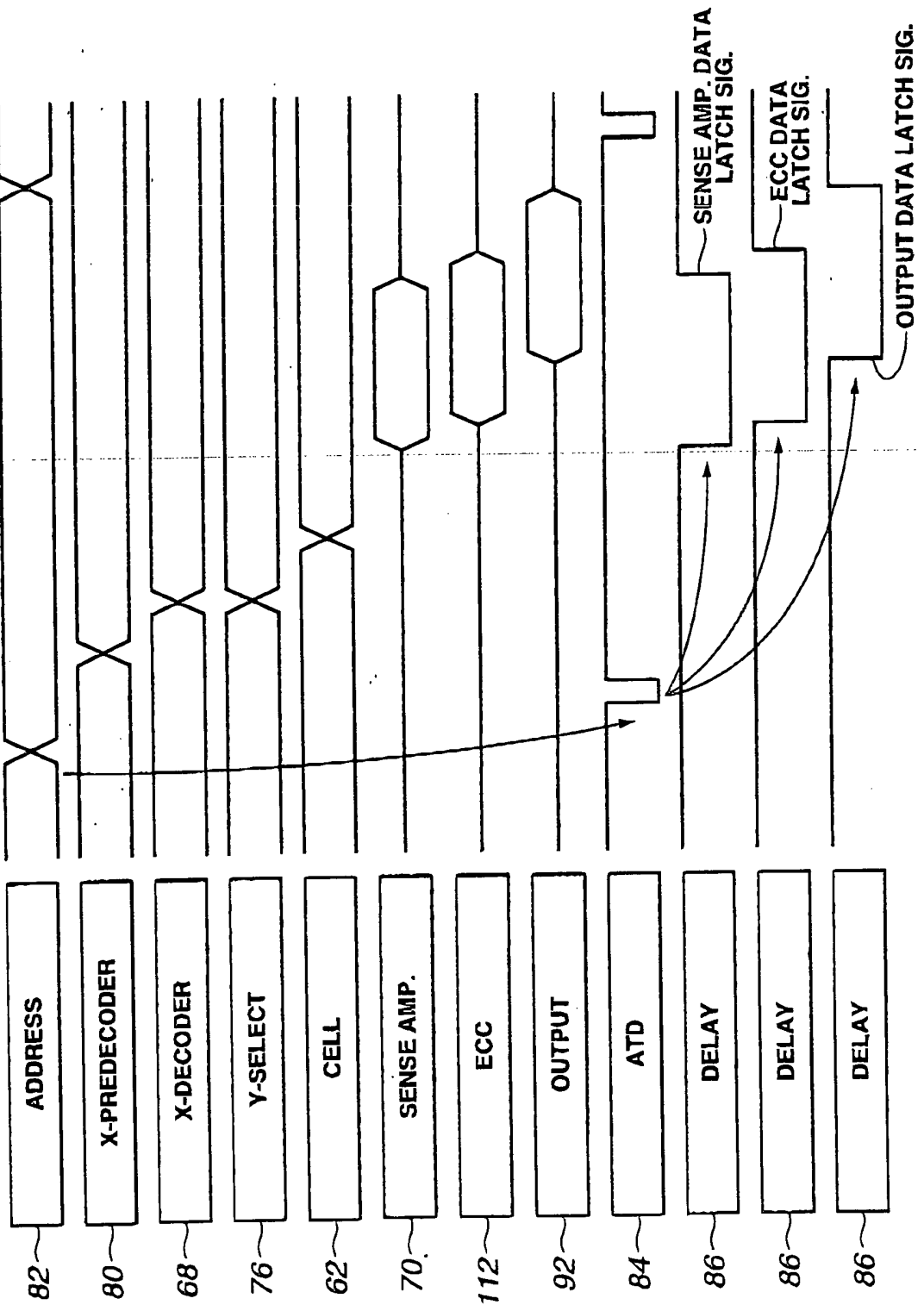

ADDRESS
X-PREDECODER
X-DECODER
Y-SELECT
CELL
SENSE AMP.
OUTPUT
ATD
DELAY
DELAY
SENSE AMP. DATA LATCH SIG.
OUTPUT DATA LATCH SIG.
82
80
68
76
62
70
92
84
86
86

FIG.7


ADDRESS
X-PREDECODER
X-DECODER
Y-SELECT
CELL
SENSE AMP.
ECC
OUTPUT
ATD
DELAY
DELAY
DELAY
SENSE AMP. DATA LATCH SIG.
ECC DATA LATCH SIG.
OUTPUT DATA LATCH SIG.
82
80
68
76
62
70
112
92
84
86
86
86